REMARKS

The Abstract of the disclosure is objected to for reasons stated in the Office Action. The Abstract is amended in a manner that is believed to overcome the objection. Entry of the amendments to the Abstract and removal of the objection are respectfully requested.

Claims 14-16 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The claims are amended above in a manner believed to overcome the rejections. In particular, independent claim 14 is amended to clarify that data transmitted to a global read line pair is transmitted through a data output (input) pad during a read operation. Removal of the rejections of claim 14, and claims 15-16 dependant thereon, are respectfully requested.

Applicants note with appreciation that the Office Action at page 10 indicates that claims 6, 7, 9, 10, and 13 would be allowable if rewritten in independent form. Accordingly, independent claim 4 is amended to include the limitations of original claim 7, and claim 7 is canceled. Independent claim 8 is amended to include the limitations of original claim 9, and claim 9 is canceled. Independent claim 11 is amended to include the limitations of original claim 13, and claim 13 is canceled. New claim 17 is claim 6 rewritten in independent form. New claim 19 is claim 10 rewritten in independent form. Entry and allowance of allowable amended independent claims 1, 4, 8, and 11, and dependent claims thereon, and new independent claims 17 and 19, and dependent claims thereon, are respectfully requested.

Applicants further note that the Office Action at page 10, second paragraph indicates that claim 16 would be allowable if rewritten to overcome the rejection under 35 U.S.C. 112, second paragraph. In view of the amendments to independent claim 14, from which original claim 16 depended, it is submitted that the rejection under 35 U.S.C. 112, second paragraph, is overcome. Further, independent claim 14 is amended to include the allowable limitations of original claim 16, and claim 16 is canceled. Entry and allowance of amended independent claim 14, and claim 15 dependent thereon, are respectfully requested.

Claims 1-5, 11, 12, 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by

Osada, *et al.* (United States Patent No. 6,665,209) or Hidaka (United States Patent No. 6,542,428) or Watanabe, *et al.* (United States Patent No. 6,418,067). Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka in view of Watanabe, *et al.* As described above, independent claim 4 is amended to include the limitations of original claim 7, independent claim 8 is amended to include the limitations of original claim 9, independent claim 11 is amended to include the limitations of original claim 13, and independent claim 14 is amended to include the limitations of original claim 16. Therefore, independent claims 4, 8, 11, and 14 are believed to be allowable, and reconsideration of the rejections of amended independent claim 4 and claim 5 dependent thereon, independent claim 8, independent claim 11 and claim 12 dependent thereon, and independent claim14 and claim 15 dependent thereon, is respectfully requested.

With regard to the rejection of independent claim 1, the present invention as claimed in amended independent claim 1 is directed to a semiconductor device comprising a memory cell array, a predetermined number of write line pairs, a predetermined number of read line pairs, a data input circuit, a plurality of write column selection gates, a plurality of read column selection gates, and a data output circuit. The memory cell array includes a plurality of memory cells connected between a plurality of word lines and a plurality of bit line pairs. The data input circuit transmits first data which is applied through data input pads to the predetermined number of write line pairs as second data during a write operation. The plurality of write column selection gates receive the first data from the data input circuit and transmit the second data between the plurality of bit line pairs and the predetermined number of write line pairs during the write operation. The plurality of read column selection gates transmit third data between the plurality of bit line pairs and the predetermined number of read line pairs during a read operation. The data output circuit outputs the third data as fourth data during the read operation. The fourth data is output through data output pads. The first data is input through the data input pads during the write operation and the fourth data is output through the data output pads during the read operation simultaneously.

These features of the claimed present invention are illustrated at least at Figures 1 and 3

of the present specification. In this example, data input circuit 16 transmits first data DI11-DI14 which is applied through data input pad DQI to write line pairs LW11/B-LW14/B as second data di1 via global write line pairs GW1/B-GW4/B during a write operation (see page 14, lines 14-18 of the present specification). Write column selection gate WYG11 transmits the data di1 between write line pairs LW11/B-LW14/B and sense bit line pairs SBL1/B-SBL4/B and array bit line pairs BL1/B- BL4/B during the write operation (see page 15, lines 3-6 of the present specification). Read column selection gate RYG11 transmits third data d01 from bit line pairs SBL1/B, SBL2/B to read line pairs LR11/B, LR11/B during a read operation, wherein data output circuit 18 outputs the third data as fourth data DO11-DO14, wherein the fourth data is output through data output pad DQO (see page 14, lines 8-12 of the present specification). In this manner, the first data DI11-14 is input through the data input pad DQI during the write operation and the fourth data DO11-DO14 is output through the data output pad DQO during the read operation simultaneously (see page 14, lines 19-21 of the present specification).

Claim 1 is amended herein to clarify certain features of the present invention. In particular, claim 1 is amended to clarify that a data input circuit transmits first data through data input pads to a predetermined number of write line pairs as second data during a write operation. In addition, claim 1 is amended to clarify that a plurality of write column selection gates receive a first data from a data input circuit and transmit second data between a plurality of bit line pairs and a predetermined number of write line pairs during a write operation. In addition, claim 1 is amended to clarify that a plurality of read column selection gates transmit third data between a plurality of bit line pairs and a predetermined number of read line pairs during a read operation. In addition, claim 1 is amended to clarify that a data output circuit outputs third data as fourth data during a read operation, wherein the fourth data is output through data output pads. In addition, claim 1 is amended to clarify that first data is input through data input pads during a write operation and fourth data is output through data output pads during a read operation simultaneously.

With regard to the rejection of claim 1 based on Osada, *et al.*, it is submitted that Osada, *et al.* fails to teach or suggest first data that is input through data input pads during a write

operation and fourth data is that is output through data output pads during a read operation simultaneously, as claimed in claim 1. Moreover, there is no teaching or suggestion in Osada, *et al.* of a data input circuit for transmitting first data which is applied through data input pads to a predetermined number of write line pairs as second data during a write operation, nor is there any teaching or suggestion in Osada, *et al.* of a data output circuit for outputting third data as fourth data during a read operation, wherein the fourth data is output through data output pads, as claimed. Osada, *et al.* teaches a write amplifier circuit 102 having an input IN and a latch circuit 104 having an output OUT (see Osada, Figure 1). Osada, *et al.* further discloses that read and write operations can be completed in a clock cycle (see Osada, column 4, lines 6-9). However, close inspection of Osada, *et al.* reveals that there is no mention of the write amplifier circuit 102 of Osada, *et al.* transmitting first data which is applied through data input pads during a write operation, and there is no mention in Osada, *et al.* of the latch circuit 104 outputting third data as fourth data during a read operation, the fourth data being output through data output pads, wherein the first data is input through the data input pads during the write operation and the fourth data is output through the data output pads during the read operation simultaneously. It therefore follows that the write amplifier circuit 102 Osada, *et al.* is not a data input circuit, as claimed, and that the latch circuit 104 of Osada, *et al.* is not a data output circuit, as claimed.

For these reasons, it is submitted that Osada, *et al.* fails to teach or suggest the present invention, as claimed in amended independent claim 1. Reconsideration and removal of the rejection of claim 1, and claims 2-3 dependent thereon, under 35 U.S.C. 102(e) based on Osada, *et al.* are respectfully requested.

With regard to the rejection of claim 1 based on Hidaka, it is submitted that Hidaka fails to teach or suggest first data that is input through data input pads during a write operation and fourth data that is output through data output pads during a read operation simultaneously, as claimed in claim 1. Hidaka discloses an I/O buffer 85 coupled to a data input terminal 15 and a data output terminal 17 (see Hidaka, Figure 1). However, there is no teaching or suggestion in Hidaka of the I/O buffer 85 transmitting first data which is applied through data input pads during a write operation, and there is no teaching or suggestion in Hidaka of the I/O buffer 85

outputting third data as fourth data during a read operation, the fourth data being output through data output pads, wherein the first data is input through the data input pads during the write operation and the fourth data is output through the data output pads during the read operation simultaneously. Thus, it follows that the I/O buffer 85 of Hidaka is neither a data input circuit, as claimed, nor a data output circuit, as claimed.

For these reasons, it is submitted that Hidaka fails to teach or suggest the present invention, as claimed in amended independent claim 1. Reconsideration and removal of the rejection of claim 1, and claims dependent thereon, under 35 U.S.C. 102(e) based on Hidaka are respectfully requested.

With regard to Watanabe, *et al.*, it is submitted that Watanabe, *et al.* fails to teach or suggest first data that is input through data input pads during a write operation and fourth data that is output through data output pads during a read operation simultaneously, as claimed in claim 1. Watanabe, *et al.* teaches data input buffers DB0-DB1 and data output buffers QB0-QB31 (see Watanabe, Figure 7). However, there is no teaching or suggestion in Watanabe, *et al.* of the data input buffers DB0-DB1 transmitting first data which is applied through data input pads during a write operation, and there is no teaching or suggestion in Watanabe, *et al.* of the data output buffers QB0-QB31 outputting third data as fourth data during a read operation, the fourth data being output through data output pads, wherein the first data is input through the data input pads during the write operation and the fourth data is output through the data output pads during the read operation simultaneously. Thus, it follows that the data input buffers of Watanabe, *et al.* are not a data input circuit, as claimed. It further follows that the data output buffers of Watanabe, *et al.* are not a data output circuit, as claimed.

For these reasons, it is submitted that Watanabe, *et al.* fails to teach or suggest the present invention, as claimed in amended independent claim 1. Reconsideration and removal of the rejection of claim 1, and claims dependent thereon, under 35 U.S.C. 102(e) based on Watanabe, *et al.* are respectfully requested.

In view of the amendments to the specification and the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such

allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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